CLAIMS:

1. A data processing circuit switchable between operation in a cache mode and a cache bypass mode, the data processing circuit comprising a power supply connection, a cache memory and a power supply switch coupled between the power supply connection and a power supply input of the cache memory, the power supply switch cutting off power supply to the cache memory when the data processing circuit operates in the cache bypass mode.

2. A data processing circuit, comprising

- a processor circuit for executing program instructions;
- a memory interface for communicating with a main memory;
- a cache memory;
- a power supply connection;
- a power supply switch coupled between the power supply connection and a power supply input of the cache memory;
- a cache interface circuit coupled to the processor circuit, the memory interface, the cache memory and a control input of the power supply switch, and arranged to switch between a cache mode and a cache bypass mode in response to an instruction executed by the processor circuit, the cache interface circuit causing information read from the memory interface in response to a memory reading instruction from the processor to be cached in cache memory for reuse in response to further memory reading instructions in the cache mode, the cache interface circuit servicing all memory reading instructions from the processing circuit by means of access to main memory interface in the cache bypass mode, the cache interface circuit controlling the power supply switch to supply power to the cache memory in the cache mode and to cut off power supply to the cache memory when operating in the bypass mode.

3. A data processing circuit switchable between operation in a cache mode and a cache bypass mode, the data processing circuit comprising

- a processor circuit for executing program instructions;
- a memory interface for communicating with a main memory;

- a cache memory, the processing circuit servicing memory reading instructions from the cache memory in the cache mode, the processing circuit bypassing the cache for all memory reading instructions in the cache bypass mode;
- a power supply connection;
- a power supply switch coupled between the power supply connection and a power supply input of the cache memory, the power supply switch cutting off power supply to the cache memory in the cache bypass mode.

4. An apparatus that contains
- a data processing circuit switchable between operation in a cache mode and a cache bypass mode, the data processing circuit comprising a power supply connection, a cache memory and a power supply switch coupled between the power supply connection and a power supply input of the cache memory, the power supply switch cutting off power supply to the cache memory when the data processing circuit operates in the cache bypass mode
- a medium containing a program for the data processing circuit, the program containing a first and a second portion, and instructions for switching between the cache mode and the cache bypassing mode, so that the first portion is executed in the cache mode and the second portion is executed in the cache bypass mode, wherein execution of the first portion would not meet a real time constraint for operation of the apparatus if the first portion were executed in the cache bypass mode.

5. A computer program product containing the program for the apparatus of Claim 4.